12.1 A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO

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In the deep submicron era, analog circuits suffer from an insufficient voltage headroom, leakage current, and lack of portability. Although there have been attempts to make digital CDR circuits [1, 2], those approaches still require analog phase interpolators or multi-phase clock generators. In this paper, an all-digital multi-gigabit CDR circuit that uses a 10b monotonic DCO is presented. The CDR exhibits 7.2ps$_{rms}$ jitter at 2.5Gb/s and operates down to 0.9V supply.

The block diagram of the receiver architecture is shown in Fig. 12.1.1. The receiver is composed of a bang-bang phase detector (BBPD), a DCO, a 1:8 deserializer (DES), and fully synthesized control logic. Only the 1:8 DES is manually routed to meet coupling and loading requirements. The routing of the DCO is sufficiently regular to allow automatic placement and routing using the matrix technique. A conventional BBPD samples the input data at the center and edge of the data transition. Since fully synthesized control logic is hard to operate at the input data rate, the data is deserialized by the DES. After that, 16b from the DES are fed into the control logic to produce a (32+31)b thermometer code for frequency tuning. In order to achieve loop stability, an additional 2b forward path connects the BBPD directly to the DCO. The control logic and the forward path replace the charge pump and RC loop filter in charge-pump PLL.

The fully synthesized control logic is made up of an UP/DN generator, an IIR filter, a ΔΣ modulator, a binary-to-segmented thermometer converter (B2T), and a frequency detector (FD). The UP/DN generator produces the UP/DN information (-8 to +8) from the 16b that are sampled at the center and edge of the input data transition. The IIR filter is a simple 1st-order integrator with 17b resolution; it integrates the UP/DN information and generates a 17b frequency code. Since it would be hard to design a DCO with 17b resolution, the 1st-order ΔΣ modulator takes the 17b frequency code as an input and dithers between 2 successive 10b control codes, which effectively provides 17b-resolution frequency tuning from a 10b-resolution DCO. The code converter then converts the 10b binary control code into the 2 thermometer codes required by the segmented thermometer scheme. The FD is used to set the initial frequency code at power-up until the frequency lock is detected, ensuring that the frequency of the DCO is inside the capture range of the loop. The FD estimates the frequency difference by counting the transitions of the reference clock, which is 1/64 frequency of the input data rate. All components of the fully synthesized logic operate with the output clock of the DES, which is 1/8 frequency of the input data rate.

The DCO shown in Fig. 12.1.2, is a 3-stage inverter chain with its power supply connected through a digitally controlled resistor. This resistor is made up of 1024 PMOS transistor switches that are used for frequency tuning and 96 switches that control the initial oscillation at power-up. Thermometer control is preferred to binary control for preventing these switches from causing glitches during the control code transitions [3]. On the other hand, binary control requires less routing area. In this design a segmented thermometer scheme is adopted to obtain the advantages of both approaches [4]. The proposed scheme uses only 32+31 routing wires to control 1024 switches. To eliminate glitches at the row boundaries, the control code should only turn one switch on or off at a time (Fig. 12.1.3). A cell in an even row is turned on when the corresponding column code is 1 and a cell in an odd row is turned on when the corresponding column code is 0. In addition, a cell in the first column is turned on when the corresponding row code is 1.

The DCO has 16 additional tuning cells for the 2b forward path that receive the UP/DNb signal from the BBPD. These cells directly control the frequency of the DCO at a speed that is 8-times higher than the integral path to provide stability. The extent of this forward tuning should be no more than is necessary to provide sufficient stability. The DCO is therefore designed so that one UP/DNb turns on or off between 1 and 8 tuning cells, depending on C_{PROP}[2:0]. Additionally, the extent of the integration tuning by the IIR filter is controlled by setting the coefficient C_{INT} that changes the bandwidth of the loop.

In the design of the DCO, the tuning steps ($f_{step}=f_{n+1}/f_n$) should be as even as possible in order to maintain the designed loop stability and bandwidth [5]. Equally spaced tuning steps mean that the frequency increases exponentially ($f_n=f_0 f_{step}^{\ n}$) as the control code increases. However, achieving an exponential relationship by sizing 1024 switches is too awkward, and is also inappropriate for automatic placement and routing. Instead, PMOS transistors that act as resistors are inserted between the rows (Fig. 12.1.2). This produces an overall resistance change that is close to an exponential, and the frequency can also be tuned exponentially for a change of the row code. Since this is not true for a change of the column code, the frequency step has discontinuity at the row boundary. Figure 12.1.4 shows the measurement of these characteristics. As described above, the control code has the exponential relationship to the DCO frequency. The frequency step (f_{n+1}/f_n) is almost constant (0.2%) except near the control limit, but has discontinuity at the row boundary or with a period of multiple of 32. Figure 12.1.5 shows the frequency spectrum of the recovered clock. The tuning resolution of the center frequency is ~8ppm, which is a consequence of the 17b resolution of the IIR filter. However, since the resolution is achieved by dithering, the dithering frequency is appeared as a spur. In Fig. 12.1.5, this spur appears 312.5MHz away from the center frequency because the operating clock frequency of the dithering logic is 1/8 of the input data-rate of 2.5Gb/s. These quantization effects are converted to the jitter in the time domain. Figure 12.1.5 shows the measured jitter of the recovered clock using a PRBS of 2^{31}-1 at 2.5Gb/s with a 1.2V supply. The jitter is measured to be 7.2ps$_{rms}$ and 47.2ps$_{pp}$, which is low enough for multi-gigabit transceivers.

Since the CDR is purely digital, it can operate at a lower supply voltage. In addition, the loop bandwidth solely determined by the integral coefficient, is not affected by the supply-voltage variation. Figure 12.1.6 shows the operational supply voltage and the maximum data rate at each voltage. The fact that the CDR operates up to 1.35Gb/s at 0.9V supply, indicates that the proposed architecture can be adopted in deeper process without any modification.

The CDR circuit with an ADPLL is fabricated in a 0.13μm CMOS process and dissipates 13.2mW at 2.5Gb/s from a 1.2V supply. A micrograph of the die is shown in Fig. 12.1.7. The 300×430μm^2 chip has an active area of 0.08mm^2.

References:

[1] S. Sidiropoulos and M. A. Horowitz, "A Semidigital Dual Delay-Locked Loop," *IEEE J. Solid-State Circuits*, vol.32, pp. 1683-1692, Nov., 1997.

[2] B.J. Lee, M. Hwang, J. Kim, et al., "A Quad 3.125Gb/s Transceiver Cell with All-Digital Data Recovery Circuits," *Symp. VLSI Circuits Dig.*, pp. 384-387, Jun., 2005.

[3] T. Olsson and P. Nilsson, "A Digitally Controlled PLL for SoC Applications," *IEEE J. Solid-State Circuits*, vol.39, pp. 751-760, May, 2004.

[4] J. A. Shoeff, "An Inherently Monotonic 12 bit DAC," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 6, pp. 904-911, Dec., 1979.

[5] A. Maxim, B. Scott, E.M. Schneider, et al., "A Low-Jitter 125-1250 MHz Process-Independent and Ripple-Poleless 0.18μm CMOS PLL Based on a Sample-Reset Loop Filter," *IEEE J. Solid-State Circuits*, pp. 1673-1683, Nov., 2001.

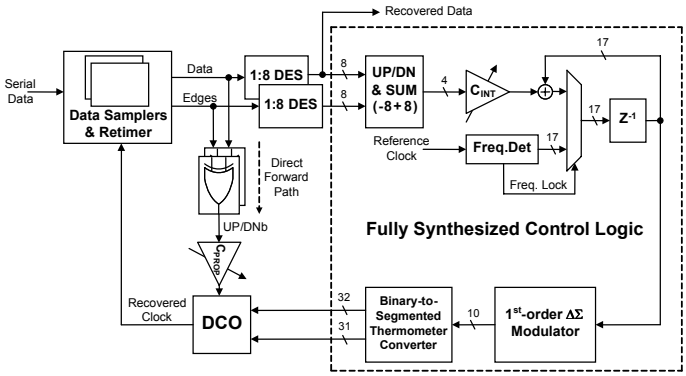


Figure 12.1.1: Overall block diagram.

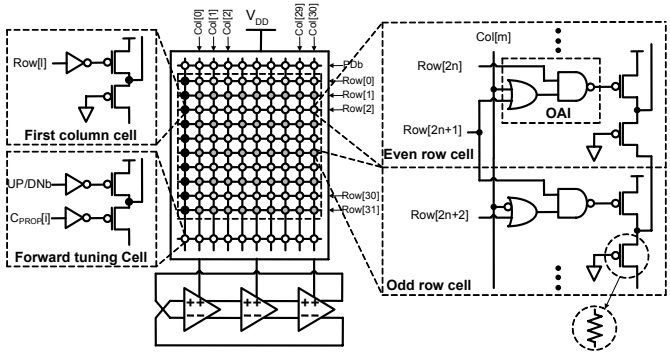


Figure 12.1.2: Schematic of the DCO.

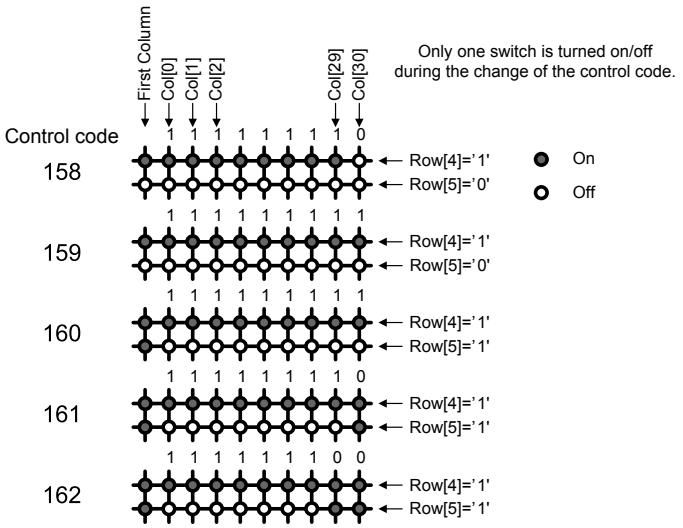


Figure 12.1.3: Control code changes at row boundaries.

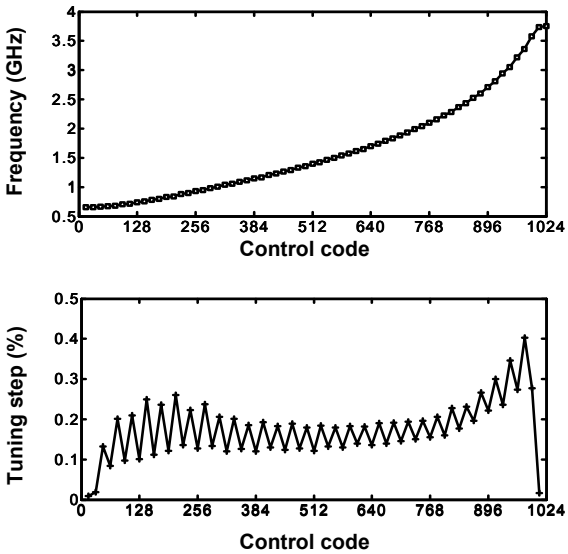
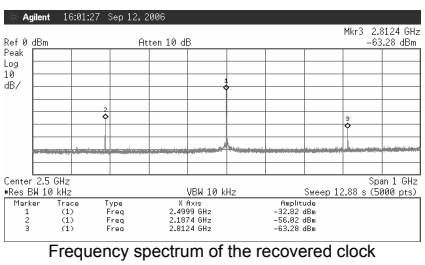
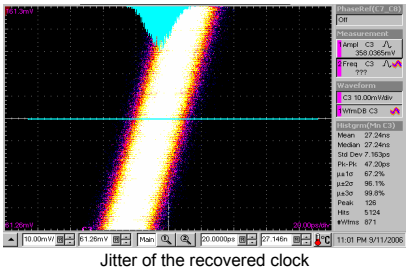


Figure 12.1.4: Measured frequency characteristics of the DCO.



Frequency spectrum of the recovered clock



Jitter of the recovered clock

Figure 12.1.5: Measurement result of the recovered clock at 2.5Gb/s.

CDR	
Technology	0.13μm CMOS
Supply Voltage	0.9 to 1.2V
Maximum data rate	1.35Gb/s @ 0.9V
	1.95Gb/s @ 1.0V
	2.42Gb/s @ 1.1V
	2.87Gb/s @ 1.2V
Power consumption	13.2mW @ 2.5Gb/s, 1.2V
Jitter @ 2.5Gb/s, 1.2V	$7.2ps_{rms}$, $47.2ps_{pp}$
Area	$0.13mm^2$
DCO	
Resolution	10b (=0.2%)
Number of control bits	31 (row) + 32 (column) + 2 (UP/DNb) + 1 (PDb) = 66b
Tuning range	0.66 to 3.7GHz @ 1.2V
Dithering frequency	1/8 of the DCO frequency
Power consumption	2.4mW @ 2.5Gb/s, 1.2V

Figure 12.1.6: Summary of circuit characteristics.

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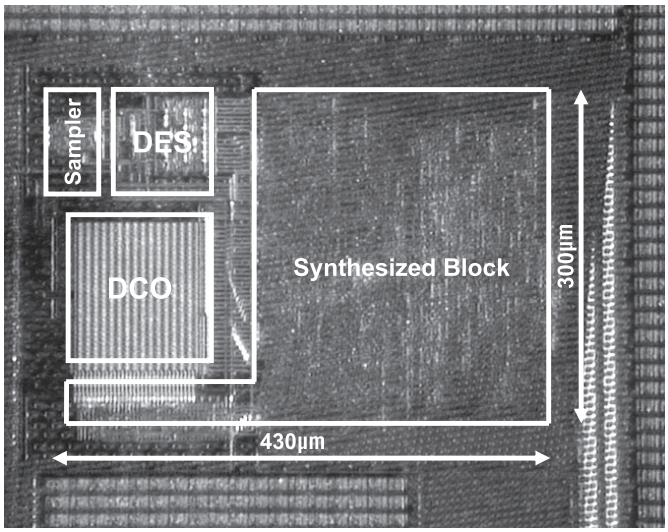

Figure 12.1.7: Die micrograph.

